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DESIGN OF EFFICIENT COMPARATOR USING MAJORITY LOGIC FORMULATION

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Abstract: Majority gate and inverter are the basic logic units of Quantum-dot Cellular Automata circuits. Most former comparators are designed in three-input majority gates and inverters. In this paper, a design of efficient comparator using majority logic formulation is presented. The proposed comparator is simulated in QCA Designer and the result shows that the logic function of proposed comparator is better in all aspects.

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I INTRODUCTION

In VLSI had been achieved on 3 factors: Area, Power and Timing (Speed).Area optimization manner decreasing the space of common sense which occupy on the die. This is accomplished in both the front-quit and lower back-end of layoutQuantum-dot cell automata (QCA) are an attractive rising technology suitable for the improvement of extremely dense low-power high-performance digital circuits. Quantum-dot cell automata (QCA) which employs array of coupled quantum dots to put in force Boolean good judgment function. The benefit of QCA lies in the extraordinarily excessive packing densities viable because of the small size of the dots, the simplified interconnection, and the extraordinarily low electricity put off product. A fundamental QCA cellular consists of 4 quantum dots in a rectangular array coupled by way of tunnel obstacles. Electrons are capable of tunnel between the dots, but cannot leave the mobile. If two excess electrons are placed within the mobile, Coulomb repulsion will force the electrons to dots on opposite corners. There are as a result energetically equal ground country polarizations can be labelled common sense "zero"and "1".The primary constructing blocks of the QCA structure are AND,OR and NOT. By the use of the Majority gate we will lessen the quantity of put office by using calculating the propagation and generational consists of.

Quantum dots are semiconductors restrained in all three dimensions of space or alternatively, it may be stated that Quantum dot is a simple fee box and it's far three dimensionally constrained [8]. The promising opportunity of CMOS paradigm is the Quantum dot cell Automata (QCA) that is used to symbolize the facts in binary M' and binary 'O' in terms of electronic price configuration. In 1993, C. S. Lent et al. First brought the theoretical Quantum dot Cellular Automata [3] and in early 1999, C. S. Lent et al. Described the experimental approach to design QCA cell with Gas [8]. The dynamic behaviour of QCA become discussed with the assist of the hart tree approximation [4], Quantum mechanics is also involved in finding out the mobile size and dot radius of a unmarried QCA cell. Hence, QCA have become research hobby to establish as robust CMOS alternative. During ultimate many years, in nanotechnology era, an exhaustive studies has been completed in this area. QCA remains in infancy stage, desires masses of study for QCA good judgment circuit layout. The low strength reversible common sense circuit design, tile based good judgment circuit design in addition to its defect analysis are prime

Columbic repulsion will reason the electrons to occupy handiest the corners of the QCA cellular resulting in unique polarizations. Electron tunnelling is assumed to be completely controllable via capability limitations (that would

exist underneath the cell) that can be raised and diminished between adjoining QCA cells by way of capacitive plates.

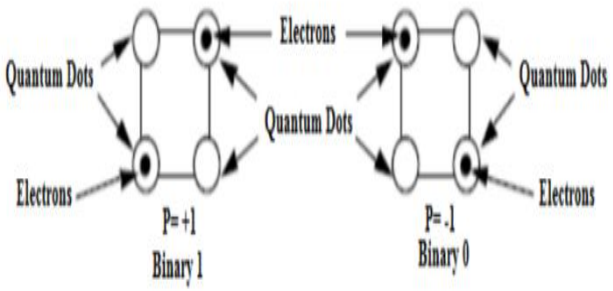


Figure 1. QCA cell polarizations and representations of binary 1 and binary 0.

For an remote cellular there are two energetically minimum equal arrangements of the two electrons within the QCA mobile, denoted mobile polarization P = +1 and mobile polarization P = -1. Cell polarization P = +1 represents a binary 1 whilst mobile polarization P = -1 represents a binary zero. This concept is likewise illustrated graphically in Figure 2. It is also worth noting that there may be an unpolarised country as well. In an unpolarised country, inter-dot potential limitations are decreased which reduces the confinement of the electrons on the person quantum dots. Consequently, the cells exhibit little or no polarization and the twoelectron wave capabilities have delocalized throughout the cell [133] as shown in Figure 2.

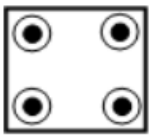


Figure 2. QCA Unpolarized Cell

The numbering of dots denoted by i inside the mobile is going clockwise starting from the dot on the pinnacle proper with i =1, bottom proper dot i =2, bottom left dot i =3, and pinnacle left dot i=four. The polarization P in a cellular is described as Where Pi denotes the digital rate at dot i. The polarization measures the price configuration i.e.The extent to which the digital charge is distributed most of the four dots.

Cell-to-Cell Response

The cellular-mobile reaction curve can be computed via solving the 2 particle Schrodinger equation . It can be visible that the cell-cellular response is fairly non-linear, which shows signal restoration. Even a slightly polarized enter cellular induces an nearly absolutely polarized output mobile.

Majority Logic Gate

The fundamental QCA logical circuit is the three-enter majority common sense gate [3] that looks in Figure 2.Four from which more complicated circuits may be constructed. The primary majority gate is obtained via placing 4 neighbouring cells adjacent to a device cellular that is inside the centre. Three of the side cells are used as inputs, at the same time as the remaining one is the output. The tool cell will continually assume the majority polarization because it's miles this polarization in which electron repulsion among the electrons in the three enter cells and the tool cell will be least.

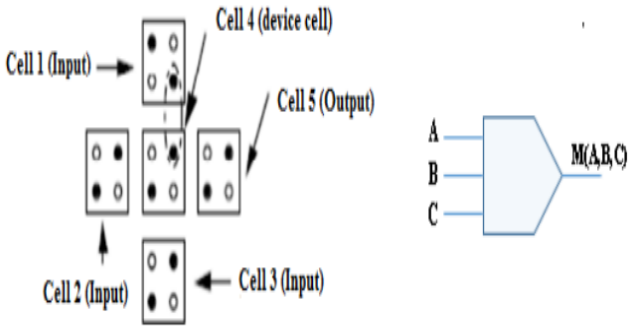


Figure 3 The Fundamental QCA Logical Device –the majority gate

To recognize how the tool cellular reaches its lowest power kingdom (and for this reason P= +1 in Figure 2), bear in mind the Coulombic interplay among cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic interaction among electrons in cells 1 and four could generally result in mobile 4 converting its polarization because of electron repulsion (assuming mobile 1 is an enter mobile). However, cells 2 and three additionally influence the polarization of cellular 4 and feature polarization P=+1. Consequently, because most people of the cells influencing the tool cell have polarization 1 P, it too will also anticipate this polarization due to the fact the forces of Coulombic interplay are more potent for it than for 1.

QCA Clocking

The clocking within the QCA circuits controls the facts go with the flow and the synchronization within the circuit. Timing in QCA is accomplished via clocking in 4 distinct and periodic levels and is wanted for each combinational and sequential circuits. Two sorts of switching strategies are feasible inside the operation of QCA: abrupt switching and adiabatic switching. In abrupt switching, the inputs to the QCA circuit change unexpectedly and the circuit can be in a few excited nation; finally, the QCA circuit is cosy to floor kingdom by means of dissipating power to the surroundings .

II LITERATURE SURVEY

The evolution of electronic facts generation (IT) and communications has been especially possible with the aid of

non-stop development in silicon-based totally Complementary Metal Oxide Semiconductor (CMOS) era. This non-stop development has been maintained often by means of its dimensional scaling, which leads to exponential boom in both tool density and performance. The discount in cost per function has regularly been growing the monetary productivity with every new era. In addition to its scalability, the specific tool homes consisting of excessive input resistance, self -isolation, 0 static electricity dissipation, and easy format and procedure steps have made CMOS transistors as the primary additives of CMOS integrated circuits (ICs).

Dimensional scaling of CMOS transistors is attaining their essential bodily limits [24-25]. Therefore, research has been actively performed to locate an alternative manner to hold to follow Moore's regulation. Among those efforts, various forms of opportunity reminiscence and good judgment gadgets, so known as "Beyond CMOS Devices," have been proposed [8]. These nandevices take advantage of the quantum mechanical phenomena and ballistic shipping characteristics underneath lower supply voltage and therefore low strength intake. These devices are expected to be used for ultra-high density incorporated digital computers because of their extraordinarily small length.

Thus, variations in Nano-twine dimensions due to fabrication imperfections can lead to perturbations in the service capacity and scattering that degrade the charge transport traits. Also, versions in Nano-wire diameters may cause a version in FET threshold voltage. Reducing variability is therefore a key mission in making Nano-wire FETs a feasible generation. Furthermore, quantum confinement consequences make modelling of Nano-cord transistors a complex trouble. The physics related to the operation of Nano-wire transistors needs to be well articulated so that easy compact fashions, which includes ballistic delivery and practical sub band parameters, can be advanced for circuit layout the use of SPICE-like simulators [33].

Carbon Nano Tubes (CNTs) were located in 1991 [34]. Due to their precise fabric properties [35], Carbon Nano Tubes (CNTs) have acquired global interest from many research works. CNTs are grapheme (that's a two-dimensional honeycomb lattice of carbon atoms) sheets rolled up into cylinders. They show both steel and semiconducting homes depending at the route how CNTs are rolled up (chirality). Since the bandgap of semiconducting CNTs is inversely proportional to their diameters, threshold voltage can be without problems controlled [36-38]. With their advanced cloth homes, including the extremely good mechanical and thermal stability, massive cutting-edge carrying potential, and high thermal conductivity, the metallic nano-tubes are attractive as future interconnects [39-41]. Along with these houses, the semiconducting nanotubes also display extremely good advantages as a channel cloth of excessive-overall performance FETs.

Single Electron Transistors (SETs) are very appealing gadgets for future largescale integration, due to their small length and coffee-strength dissipation at right pace. The primary structure of SET consists of 3-terminals: drain, gate, supply, and the second one gate, is a non-obligatory. A schematic of SET is similar to that of conventional MOSFETs. However, SET has a tiny conductive island coupled to a gate electrode with gate capacitance. Source and drain electrodes are related to the island through a tunnel barrier (junction). In SETs small voltage is implemented among the resources and drain electrodes through the "Coulomb blockade" phenomenon [42-44].

New programs and architectures that take advantage of the particular capability of room temperature operating SET circuits have been developed, specifically by using monolithic integration of SETs with FET circuits to supplement the conventional Si CMOS performance. Representative examples consist of SET/CMOS hybrid multi-price good judgment circuits [45], multiband filtering circuits [46], analog pattern matching circuits [47], associative reputation tasks [48], and others [49], wherein function Coulomb blockade oscillations of SETs are normally utilized to reduce the wide variety of gadgets. Note that sure factors of the circuit overall performance, specially the room temperature operation [39], [47-49], already exceed the theoretical assessment of the logic gate parameters for 2-nm SETs. These devices have theoretically envisioned most operation temperature T~20 K, integration density n~1011 cm-2, and pace of the order of 1 GHz [50]. However, huge threshold voltage variation continues to hinder the realization of big scale SET circuits, making it tough for SETs to compete at once with CMOS gadgets used to put into effect Boolean logic operations. Engineering breakthroughs are had to do away with the dimensions and heritage price fluctuations so as to suppress the brink voltage versions.

Single-electron tactics, representing a bit by way of a Single-electron ("bit nation common sense") [51] and using a single electron as a source of random range generations [52], have been constrained to laboratory demonstrations. The trouble of the limited fanout, that is resulting from the use of simplest an unmarried electron in the actually Single-electron gadgets, can be solved by progressive circuit designs which includes the binary selection- diagram [53]. Therefore, the deficiencies of CMOS have brought about giant efforts to locate suitable options and the various proposed answers; nano-scale technology which include Tunnelling Phase Logic (TPL), Single Electron Tunnelling (SET) and Quantum-dot Cellular Automata (QCA) have obtained giant attention [54-58].

Resent researches have proposed Quantum-dot viable implementations for QCA cells. As such Quantum-dot cells has presented in [10, 59]. An adiabatic switching paradigm is evolved for clock-managed pipelined QCA architectures. The binary statistics is saved as electronic charge main to less computing. Other investigators were extending the theoretical analysis of QCA arrays. Tonamoto et al. [60] have proposed opportunity ways of assembling QCA cells into useful gadgets. Lust and Jackson [61] have carried out graph theoretic analysis to QCA design. Chen and Pored [62] have evolved sophisticated finite element models for gate depleted Quantum-dots in semiconductors which can relate Dot occupancy to specific bias situations.

Experimental implementation of QCA in Nano-scale Metal-dot described by way of tunnel limitations has been stated in [65]. Here the authors demonstrate a managed polarization of QCA cell switching agreeing with theoretical predications. Clocked QCA operation is validated on an instance of a two cellular shift check in. In another examine [66] fan-outs are supplied.

Investigations associated with switching speed and temperature dependence of QCA have been supplied in [67]. Orthodox Coulomb blocked and grasp equation dynamic method has been considered for a semi-endless shift sign in design. The essential position of strength advantage as a feature of temperature has been shown. The conduct of such circuits as characteristic of clock speed and temperature is but to be fully explained [68]. It is found that circuit speed is limited by RC-time regular, so Majority Voters could work up to 450-diploma K, at the same time as QCA cord should paintings up to room temperatures.

The QCA bodily layout troubles were addressed in context of VLSI bodily design issues in [69]. It offers a comparison among ILP system and heuristic solution for troubles like QCA partitioning, placement and routing of QCA circuits. It has been determined that heuristic technique offers the most optimized consequences. Unidirectionality and Met stability hassle inside a QCA wire has been studied, 3Darchitecture is proposed in vicinity of uneven spacing in [70]. The classical calculation carried here has proven that 3D-configuration may also be the way to overcome Met stability problems. While H-memory is a layout evolved in particular for QCA, authors in [71] propose a new execution model that combines with Memory for dispensing the capability of CPU throughout the memory structures.

Today's QCA is nearly built as four dot cells. However, five dot or even six dot QCA designs have additionally been reported in [72]. Recent, studies studies are focusing for growing low strength devices. First time, a QCA electricity dissipation version has been proposed through Timer and Lent in [73-74] by using which common energy dissipation of an average QCA circuit is split into two primary additives, "leakage" and "switching". Power losses at some stage in clock vacillations (from low to high or excessive to low) is posited as leakage strength and energy losses in the course of switching duration is considered as switching electricity [73-75]. Numerous low strength Adder circuits with the least power dissipation have been proposed in literature [9, 76-79]. Additionally, considering fault-tolerant troubles, lots of attempts had been made to put into effect QCA fault-tolerant Full-Adder cells [80-81]. In comparison to counterpart designs the proposed Full-Adder mobile has the least power dissipation. From the complexity, latency and place point of view the proposed adder systems actually excels all the counter parts with a good sized superiority

Since on this work, both gate level method and a new explicit interplay approach had been applied for designing QCA combinational circuits. We believe that the existing research work can be of superb interest to the destiny computations.

III EXSISTING ARCHITECTURE

Majority common sense circuit consists of majority gates and inverters. Compared with the circuits designed in AND/OR/NOT gates, circuits designed in inverters and majority gates can reduce the wide variety of common sense ranges [1]. As the majority gate designed in CMOS technology is so complex that researchers begin to layout majority gate in quantum-dot cellular automata (QCA) [2-3]. Majority gate designed in QCA has extra compact structure and suggests better performance than that designed in CMOS, consequently attracting researchers' attentions. Comparator is the middle element of the virtual circuits that impacts the general performance of the complete circuit. Most present QCA comparators are designed in 3-input majority gates and inverters [4-6]. As Amara[7] proved that the usage of five-input majority gate can similarly lessen the QCA circuit common sense depth and the variety of majority gate, this paper proposes a novel layout of comparator in 5-input majority gate. The simulation indicates the logic function of the proposed comparator is accurate.

As for n-bit comparator, the outputs of one stage need to be the inputs of the next stage. For stage i, assuming the outputs are OA>B, OA

$$O^i_{A>B} = O^{i+1}_{A>B} + O^{i+1}_{A=B}F^i_{A>B}$$
$$= M_3(O^{i+1}_{A>B}, M_3(O^{i+1}_{A=B}, F^i_{A>B}, 0), 1)$$
$$O^i_{A<B} = O^{i+1}_{A>B} + O^{i+1}_{A=B}F^i_{A<B}$$
$$= M_3(O^{i+1}_{A>B}, M_3(O^{i+1}_{A=B}, F^i_{A<B}, 0), 1)$$
$$O^i_{A=B} = O^{i+1}_{A=B}F^i_{A=B} = M_3(O^{i+1}_{A=B}, F^i_{A=B}, 0)$$
$$Where\ i = (n-1, n-2 \ldots 0)$$

Proposed comparator

In this paper, we use five-input majority gates to design comparator circuit to reduce the good judgment intensity. For 1-bit comparator, the logic function of outputs can be proven as under:

$$F_{A>B} = M_5(F'_{A>B}, F'_{A>B}, M(A, \overline{B}, 0), F'_{A=B}, 0)$$
$$F_{A<B} = M_5(F'_{A<B}, F'_{A<B}, M(\overline{A}, B, 0), F'_{A=B}, 0) \quad (3)$$
$$F_{A=B} = \overline{M(M(A, \overline{B}, 0), M(\overline{A}, B, 0), 1)}$$

A, B are the inputs of the current bit while F'A>B, F'AB, YAIt is straightforward to expand the 1-bit comparator to n-bit comparator. To enhance the velocity, the proposed comparator works from each excessive bit and occasional bit. Take the 4-bit comparator for example. Assuming A3 A2 A1 A0 and B3 B2 B1 B0 are the two inputs, YA>B, YA

$$Y_{A>B} = M_5(K_1A, K_1A, K_1E, K_0A, 1)$$
$$Y_{A<B} = M_5(K_1B, K_1B, K_1E, K_0B, 1) \quad (4)$$
$$Y_{A=B} = M(K_1E, K_0E, 0)$$

The logic functions of K1A, K1B, K1E, K0A, K0B, K0E are shown as follows:

$$K_1A = M_5(M(A_3, \overline{B_3}, 0), M(A_3, \overline{B_3}, 0), M(A_2, \overline{B_2}, 0), \overline{M_3(M_3(A_3, \overline{B_3}, 0), M_3(\overline{A_3}, B_3, 0), 1), 1)}$$
$$K_1B = M_5(M(\overline{A_3}, B_3, 0), M(\overline{A_3}, B_3, 0), M(\overline{A_2}, B_2, 0), \overline{M(M(\overline{A_3}, B_3, 0), M(A_3, \overline{B_3}, 0), 1), 1)}$$
$$K_1E = \overline{M(M(M(\overline{A_3}, B_3, 0), M(A_3, \overline{B_3}, 0), 1), \overline{M(M(\overline{A_2}, B_2, 0), M(A_2, \overline{B_2}, 0), 1), 0)}}$$
$$K_0A = M_5(M(A_1, \overline{B_1}, 0), M(A_1, \overline{B_1}, 0), M(A_0, \overline{B_0}, 0), \overline{M(M(A_1, \overline{B_1}, 0), M(\overline{A_1}, B_1, 0), 1), 1)}$$
$$K_0B = M_5(M(\overline{A_1}, B_1, 0), M(\overline{A_1}, B_1, 0), M(\overline{A_0}, B_0, 0), \overline{M(M(\overline{A_1}, B_1, 0), M(A_1, \overline{B_1}, 0), 1), 1)}$$
$$K_0E = \overline{M(M(M(\overline{A_1}, B_1, 0), M(A_1, \overline{B_1}, 0), 1), \overline{M(M(\overline{A_0}, B_0, 0), M(A_0, \overline{B_0}, 0), 1), 0)}}$$

The schematic diagram of the 4-bit comparator is shown as in Figure 4

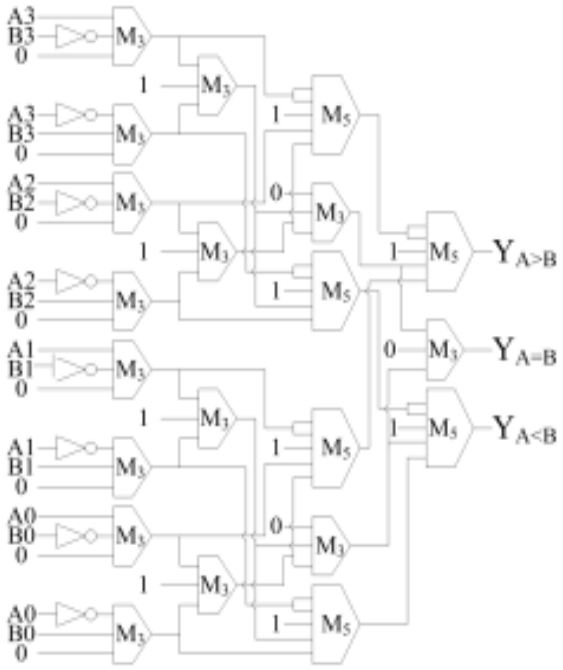


Figure 4: Schematic Diagram of the 4-bit Comparator

Proposed four-bit comparator consists of 21 majority gates and four inverters. By the use of five-input majority gate, the period of the essential path decreased. There are four majority gates at the essential route. The format of the four-bit is shown as Figure 6.

IV PROPOSED METHOD

The summed up circumstance for a comparator circuit that appears at four-bit twofold numbers an and B is given underneath:

For outlining of 4-bit comparator circuit above conditions must be executed and therefore STG Gate as AND door, STAG Gate as Full Adder, Feynman entryway as Copying entryway and NOT doors are utilized.

4-BIT COMPARATOR DESIGN: MATHAMATICAL

Proposed Four Bit Reversible Comparator Architecture Contains:

- Four STAG doors as a full viper,
- Four STG doors as reversible AND entryway,
- Two Feynman doors as a duplicating entryway and
- Ten NOT doors as an inverter. The last engineering of four piece reversible comparator is appeared in Figure 6. It can look at the estimation of two parallel numbers An and B, where A □ (A3, A2, A1, A0) and B □ (B3,B2,B1,B0) and produce the examination result as three yield signals F1,F2,F3. At the point when A □ B, F1 yield flag goes high

i.e. F1 □ FA □ B □ 1. At the point when A □ B, F3 yield flag goes high i.e. F3 □ FA □ B □ 1. At the point when A □ B, F2 yield flag goes high i.e. F2 □ FA □ B □ 1. From reproduction result as appeared in Figure 5 it is demonstrated that

• An is littler than B: F1 yield flag is high. When we apply Inputs as A3A2A1A0 □ 0000, B3B2B1B0 □ 1111 and get Outputs as F1F2F3 □ 100.

• An is equivalent to B: F2 yield flag is high. At the point when apply Inputs as A3A2A1A0 □ 1111 and B3B2B1B0 □ 1111 we get Outputs as F1F2F3 □ 010.

• An is more prominent than B: F3 yield flag is high. At the point when apply Inputs as A3A2A1A0 □ 1111 and B3B2B1B0 □ 0000 we get Outputs as F1F2F3 □ 001

Our proposed 4-bit reversible numerical comparator for the most part contains 4 MHNG entryway as full snake, and 4 three info MTG and two FG for fan-out and some not door. It can look at the estimation of two paired numbers an and B by utilizing A-B. We have demonstrated our proposed reversible numerical comparator in Fig.13.

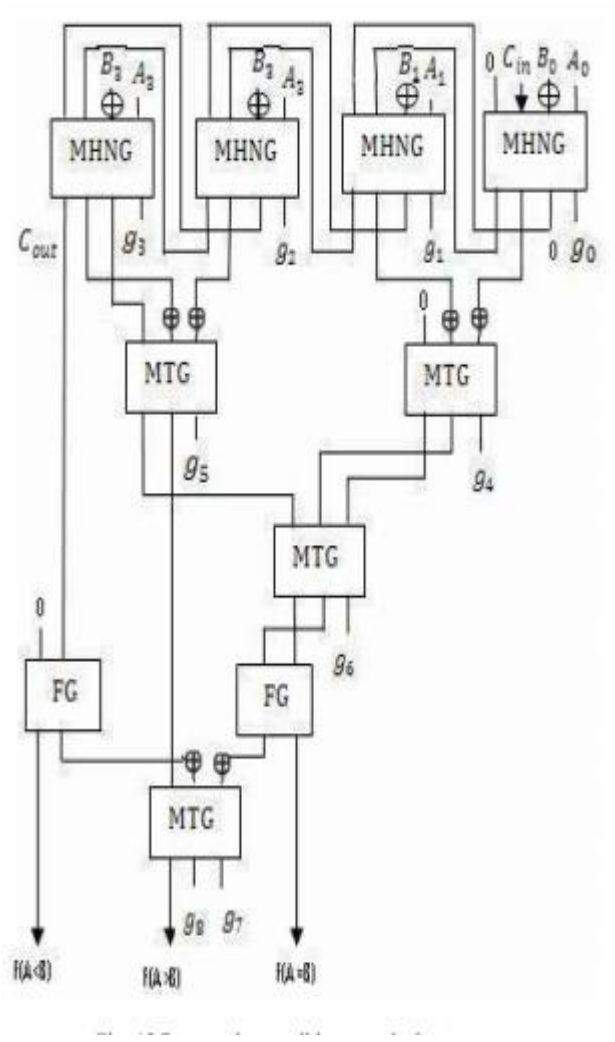
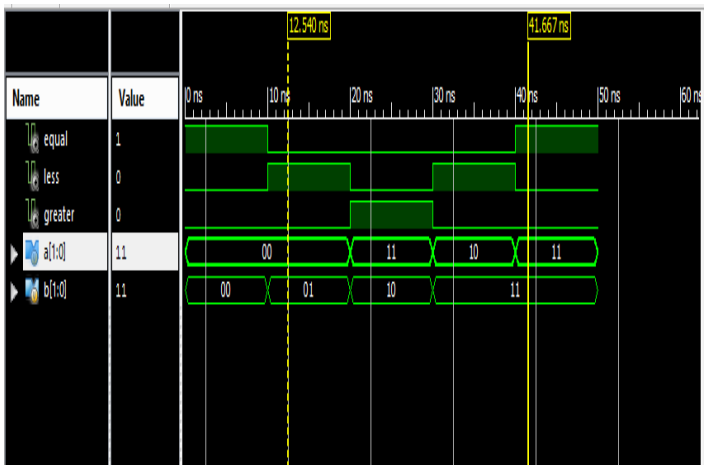


Figure 5 Proposed reversible numerical comparator

V SIMULATION RESULTS

WAVEFORMS



DESIGN SUMMARY

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	4982	204000	2%
Number of fully used LUT-FF pairs	0	4982	0%
Number of bonded IOBs	131	600	21%

The above end result represents the synthesis implementation by using the Xilinx ISE software. From the above table, it's far found that most effective 4982 look up tables are used out of available204000. It indicates very much less region (2%) was used for the proposed design.

TIME SUMMARY

```
LUT2:I0->O            1   0.043   0.000  div1/Madd_GND_49_o_GND_49_o_a
MUXCY:S->O            1   0.230   0.000  div1/Madd_GND_49_o_GND_49_o_a
XORCY:CI->O           2   0.251   0.347  div1/Madd_GND_49_o_GND_49_o_a
LUT4:I2->O            1   0.043   0.000  div1/Msub_n0258_Madd_lut<30>
MUXCY:S->O            0   0.230   0.000  div1/Msub_n0258_Madd_cy<30> (
XORCY:CI->O           1   0.251   0.289  div1/Msub_n0258_Madd_xor<31>
LUT5:I4->O            1   0.043   0.279  Mmux_out110 (out_0_OBUF)
OBUF:I->O                 0.000          out_0_OBUF (out<0>)
----------------------------------------
Total                      54.238ns (31.895ns logic, 22.343ns route)
                                    (58.8% logic, 41.2% route)
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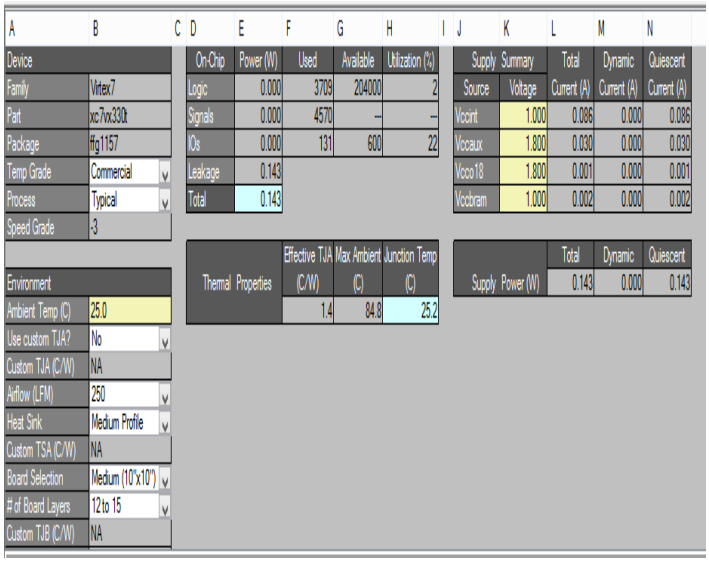
The above result represents the time consumed such as path delays by using the Xilinx ISE software. The consumed path delay is 54.238ns.

POWER SUMMARY



Device	
Family	Virtex7
Part	xc7vx330t
Package	ffg1157
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12to 15
Custom TJB (C/W)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	3709	204000	2
Signals	0.000	4570	--	--
IOs	0.000	131	600	22
Leakage	0.143			
Total	0.143			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.086	0.000	0.086
Vccaux	1.800	0.030	0.000	0.030
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.002	0.000	0.002

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.4	84.8	25.2

Supply Power (W)	Total	Dynamic	Quiescent
	0.143	0.000	0.143

The above result represents the power consumed by using the Xilinx ISE software. The consumed power is 0.143uw.

VI CONCLUSION

In this paper, we proposes a novel design of QCA comparator using five-input majority gate. The proposed comparator is simulated by QCADesigner and simulation shows the logic function of the proposed comparator is correct. Compared with previous comparator design, the proposed comparator has the least delay.

VII FUTURE SCOPE

Based on the investigation of existing structures using QCA, some of the probable future works are given below. The major performance parameters such as the number of cells, area and clock cycles provide further future work improvements of efficient digital circuits to implement using QCA. In future QCA will have a broad spotlight on strategies for proficient routing and interconnect. Apart from that, the future work in the zone of QCA framework computerization will fixate the system, to characterize timing zones.

For future adaptations of the QCA Designer, incorporating an outline standard with various design capacities such as accurate power, energy estimation, and more precise timing models improve the capability of QCA technology to reproduce the efficient digital circuits.

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