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DESIGN & COMPARISON OF NOVEL LOW POWER, SUB THRESHOLD SCHMITT TRIGGER BASED SRAM & SOURCE COUPLED LOGIC FOR COGNITIVE APPLICATIONS

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Abstract: The wide utilization & acceptance of low power devices leads to drastic growth in the miniaturization of electronic. The performance of these low power devices on par with the efficiency, But the limitations of the devices are only power and delay, as the devices are operating under the sub threshold operations. SRAM is one of the major component in digital design, occupies 50% in area and consumes nearly 40% of power. In this paper a novel sub threshold SRAM designs have proposed to improve the stability in read & write operations along with power and delay. The main focus of this research work is to address the leakage power, when the circuits are operating under the sub threshold region. The critical limitation in this design is the leakage power as the technology is increasing. As the technology increasing at a rapid rate the leakage power is dominating the dynamic power. This amount of power need to be controlled at all the levels of abstractions in the entire design. Another issue is with the delay, where this leads to reduce the speed of operation. This research work describes the two novel proposed designs which may be helpful to implement SRAM, to satisfy the above requirement. i.e. Sub threshold Schmitt trigger based SRAM & source coupled logic based SRAM. The first part of the paper describes the design and implementation of sub threshold Schmitt trigger based SRAM and analyzing the performance by write & read operations, performance through power and delay. In the second part, analysis of source coupled logic functionally and performance is analyzed and estimated, finally made a comparison between these two novel designs in power and delay under sub threshold operation. Conclusion is made based on the experimental results obtained for high frequency, low power electronics.

Keywords: *Schmitt triggered SRAM, Source coupled SRAM, Lekage power,Subthreshold operation,Designs, Bistable latch*

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I INTRODUCTION

1.1 Motivation of sub-threshold designs.

The key motivation of the sub threshold circuit design is to reduce the leakage power under sub threshold operation. As the technology evolving at a rapid rate, this power is dominating the dynamic power. Some of the other factors that are driving the sub threshold designs are power, delay, area, speed of operation portability, complexity. Lot of researchers has been focusing to reduce the leakage power under sub threshold operation as the technology is scaling down the line. [1, 2]

1.2. *Objectives of the work*

The main focus of this research paper is to offer novel low power sub threshold design techniques, that deals with sub threshold Schmitt triggered SRAM (stschSRAM), Source coupled logic based SRAM (stsclSRAM) and operating them under sub threshold region. Performance and functionality is estimated from read & write operations, and also analyzed static and dynamic power along with rise and fall time of the delay. To satisfy the above requirements & to achieve the best possible efficiency & performance by selecting the design most versatile component that consumes at least 40%-50% [3,4] of power during the operation in the overall circuit design.ie SRAM.

II RELATED WORK

2.1 Sub threshold Schmitt trigger based SRAM operation

From survey of sub threshold SRAM, it indicates that 8T SRAM is most suitable to design of SRAM. As the technology is increasing, the lambda based values are changing due to its length & width of the transistor. The design is operating under the sub threshold voltage. Whereas under the sub threshold region, the static or leakage power is dominating the dynamic power.

Therefore the predominantly the leakage power is increasing when the technology is scaling down. Therefore finally the Vth of transistor need to scale down along with lambda based dimensions. Therefore the static noise margin is increased. In this section a novel approach of Schmitt triggers based SRAM. Schmitt trigger based SRAM can be implemented with dynamic threshold metal oxide CMOS (DTMOS) techniques[5], consisting of positive feedback loop is acts as a bistable latch A separate NMOS transistor is added-between the two CMOS inverter to separate read and write operations. [6,7]. So the circuit stability can be improved [5-9]. A High Vth & low Vth transistor [6-8] are used to reduce the leakage power and finally performance is estimated by static and dynamic power along with delay.

2.1.1 Design & Operation of Schmitt trigger based SRAM

A N-type transistor of N5 is added with the existing SRAM to improve read performance & to separate the bit lines from storage nodes. P3 (P-type transistor) is added with the two cross coupled inverters to break from feedback from the read operation. Therefore the read and write operations can be Separate by word lines. Therefore it leads to an asymmetric structure. [10,11,12].

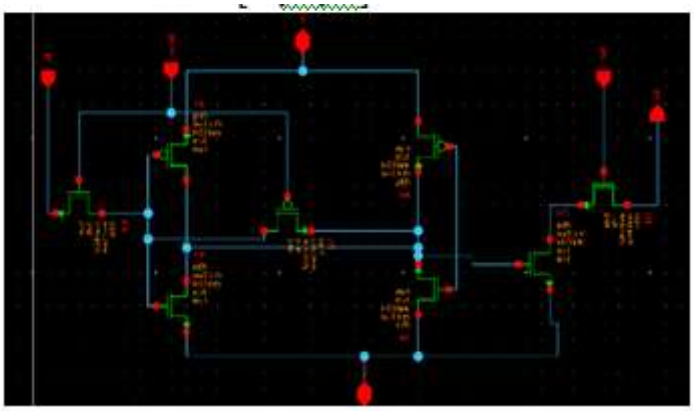


Figure 2.1 Sub threshold DTMOS based SRAM design

2.1.2 Read & write operation:

During Write operation, output carries '0' with a input of '1' at bit line. The word line has a 'high' & applied input across the BL is low. This makes the value to store in the bistable latch is '1'.

Figure 2.2 Read & write operation

Finally the bit line value bar produces the output '0'. This results in makingM3 & M4 on reading, WL is pre-charging to the bit line value to Vdd. This drives the access transistor M5 makes on & drive by Reading word line (RWL). The value stored at node Q is '0', then M7 will be on state & RBL is connected to ground, discharges through on transistors M5 & M7. Therefore the value stored at node Q is '0' & QB is 1.and vice versa as showed in fig 2.2

2.2 Power analysis

Power of analysis of the circuit is estimated by static or leakage. Where $P_{total}=P_{dynamic}+P_{static}+P_{short\text{-}circuit}$

$$Pactive=\alpha\, C_L\, Vdd^2\, F_{clk}$$

Where Vdd^2 is the supply voltage,α is an activity factor, F_{olk} clock frequency , C_L is the load capacitance. Static power is the product of leakage current with supply voltage. ie$P_{static}=V_{dd}*I_{leak}$.[11,12]

2.2.1 Static Power & Dynamic Power Dissipation

Static, total power is analyzed based on the dc input signal, where the input voltage and supply voltages are 0.4v and a threshold voltage of 0.49v . Static Power & dynamic power is as showed from the following figure 2.3 & figure 2.4.

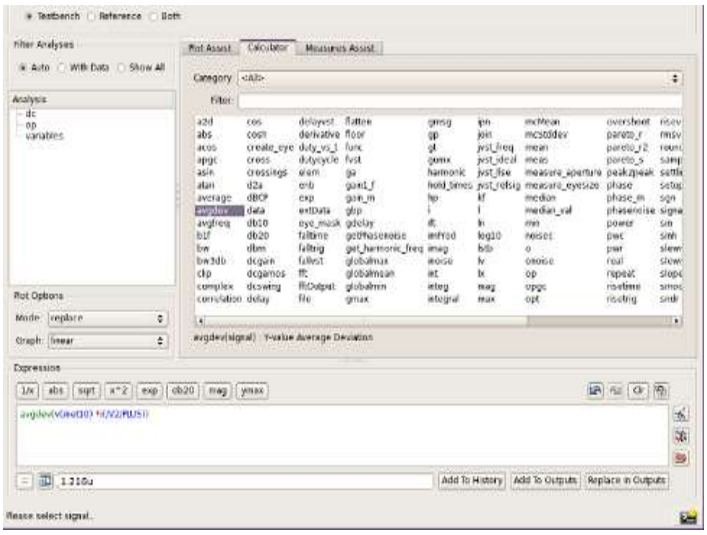


Figure 2.3 Static Power 1.216uw

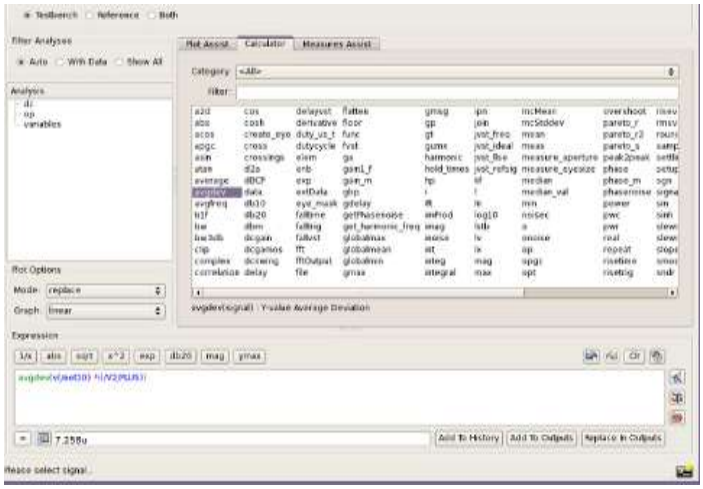


Figure 2.4 Total Power 7.258uw

2.3 Delay Analysis

The delay analysis is estimated from the rise and fall time of the characteristics

2.3.1 Rise time (t_r) & Fall time(t_f)

The time taken to raise the output signal from 10% of the maximum voltage of 90% is treated as rising time and represented by t_r,and vice versa is treated as fall time as represented by t_f. as showed from the following Figure 2.4 & Figure 2.5 And also the total time delay of the circuits is given by the 210ps.

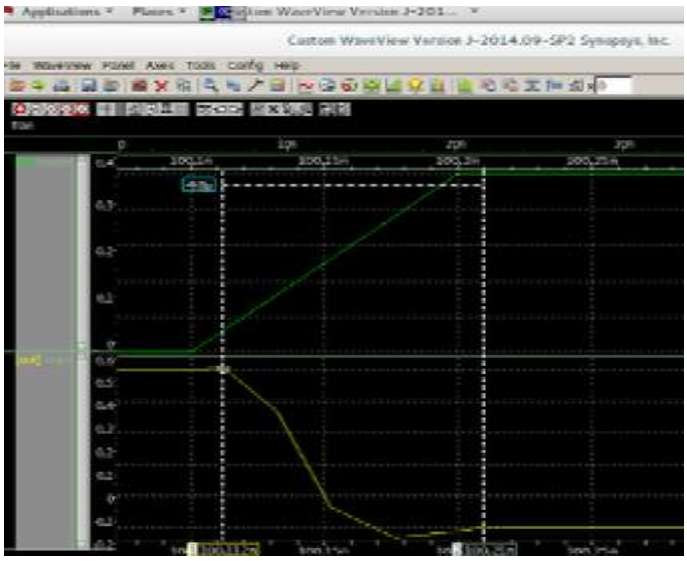


Figure 2.4 Rise time is 112 ps

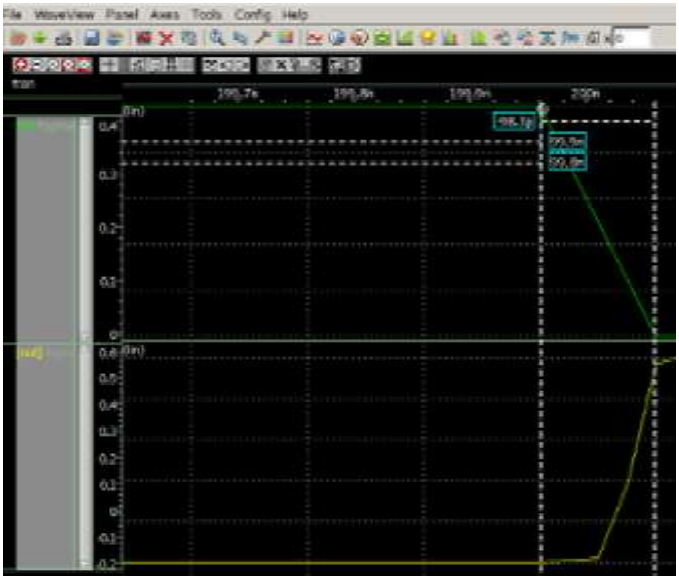


Figure 2.5 Fall time is 98ps

III NOVEL DESIGN

3.1 Novel Design of Sub threshold Source-Coupled Logic based SRAM

The second Novel design is the sub threshold source coupled logic based SRAM (ST-Scl-SRAM).The swing voltage is crucial at higher frequencies. And it is effectively maintained in SCL. Such designs are used in mixed mode and sub threshold of operation. Where noise due to subthreshold is crucial[13]. The advantage of SCL has a tail biased currents, therefore due that, less in power consumption and maximum speed. Finally maximum output voltage swing is obtained by separating the power & delay operation. Where there is a good trade-off between power, delay, supply voltage and sub threshold voltage. Therefore Power delay product (PDP) is made as successful method of SCL. The speed is depending on leakage current and independent of the supply voltage. At low activity switching, It has improved drop in delay compared to CMOS designs The tail biased current, Iss provides an opportunity to reduce the power at low switching activity too**.** The advantages of SCL are that the gates operate with minimum and supply voltages with a small logic gate depth [14]. The Problem with SCL is that they suffer from high power dissipation [9-13,14]. Some of the applications of SCL is clock data recovery circuits.

3.2 Design & Operation

A source coupled logic(SCL) design is converted into CMOS SCL by PMOS & NMOS transistors are connected in differential mode of operation as showed in below figure 3.1

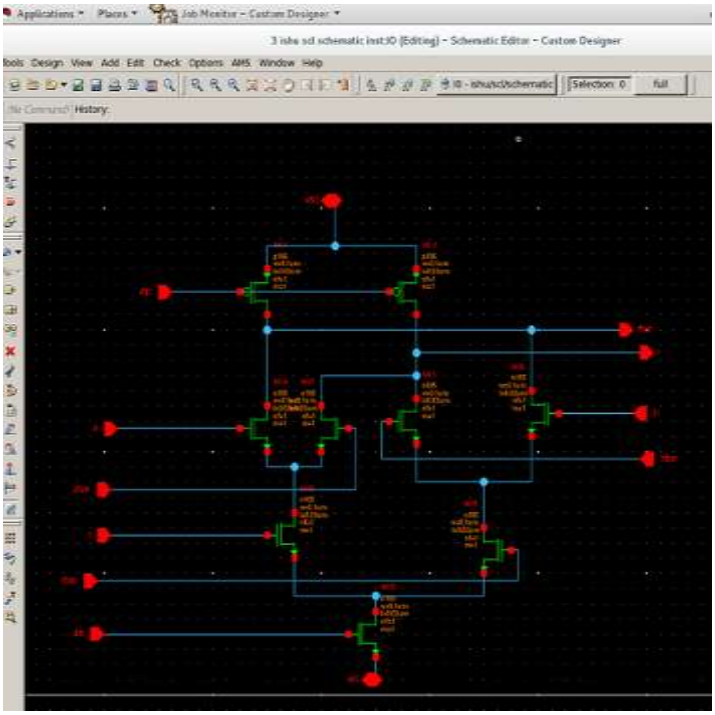


Figure: 3.1.SCL topology of Source-Coupled Logic of SRAM

Considering the input signal A is supplied with '0'v and complement of A is treated with 0.4v is the logic 1. Pmos & Nmos Transistors are acting as differential pair and produces logical value 0v & 0.4v. The first & second CMOS structure is acting differential pair with logic value of 0.4 v & 0v,0V & 0.4V During read operation BL is treated as '0'v & complement of BL are treated as '0.4' v with a supply voltage of 0.4v. The second CMOS structure operates with the 0.4v&v. This leads to high current across the NMOS transistor by considering the select

signals are 0 &1. Therefore SCL SRAM indicates the read & write operation with high & low values correspondingly.

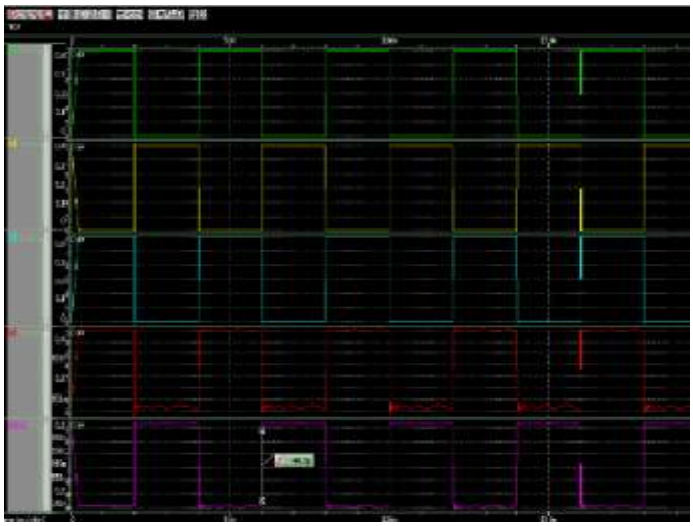


Figure: 3.2 Read & Write Operation

3.2 Power Analysis

3.2.1 Static & Total power Dissipation

The static power/leakage power across the design is estimated by applying a DC supply 0.4v& current across the design. The multiplication factor of supply voltage & current will gives static power. The static power of the source coupled logic is estimated from the following figure 3.3 & figure 3.4

Figure: 3.3 Static Power of SCL 13.55µw

The power analysis made with the voltage and current across the input & output path. The product of voltage and the current across the input is estimated, by applying a pulse with voltage values under the sub threshold operation. Therefore the dynamic power can be obtained from these inputs. The total power of the circuit is estimated by considering the static and dynamic modes of operation[15,16].Total power =T Static +T Dynamic power, Therefore Dynamic power = Total power – T Static power.

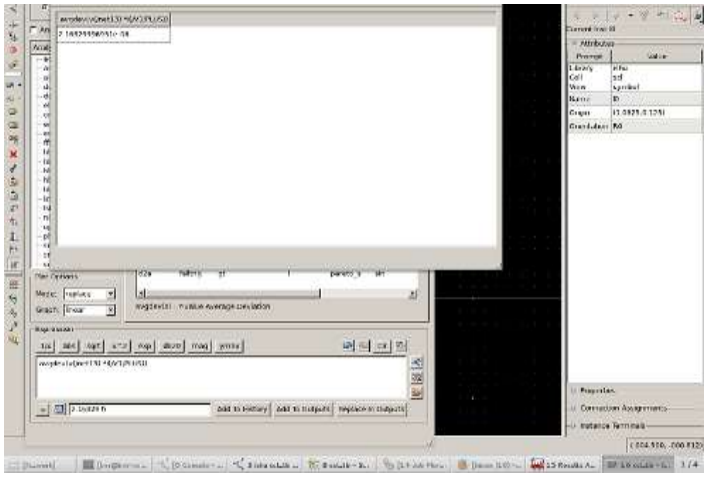


Figure 3.4 Total Power of SCL SRAM 2.16829nw

3.3 Delay Analysis

3.3.1 Rise time & fall time (t_r &t_f)

Delay is major & important factor under sub threshold operations. Delay in digital circuits is estimated from rise & fall time of the response. This can be estimated by the characteristics read and write operations. The characteristic 10% to 90% of is the rise time and is represented by 223ps, and total delay is approximated as 0.243ns showed in figure 3.5 & figure 3.6

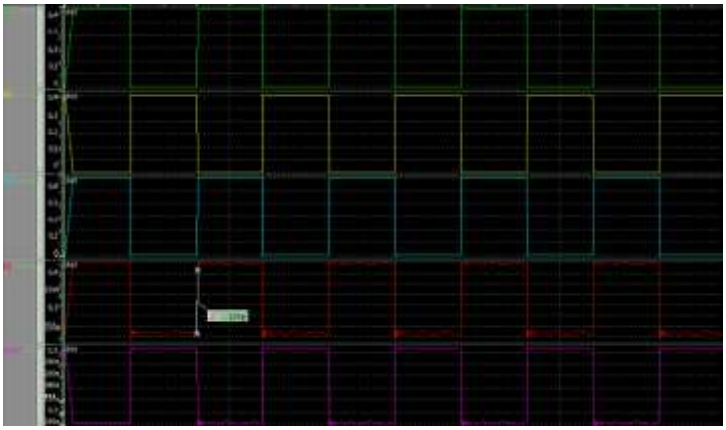


Figure: 3.5 Rise time Delay is 223 Ps

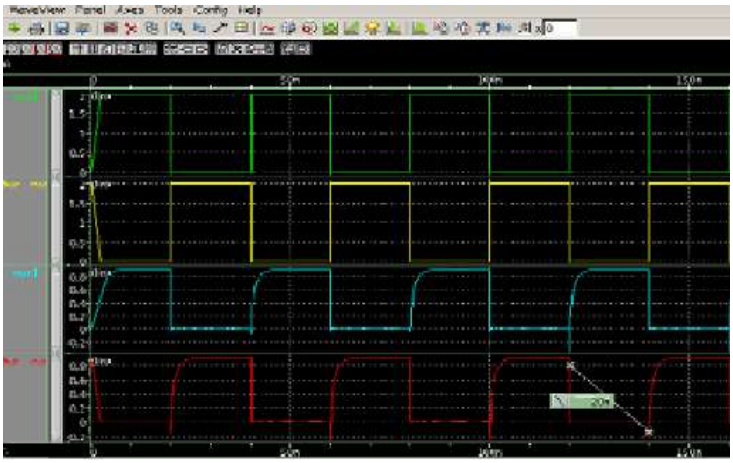


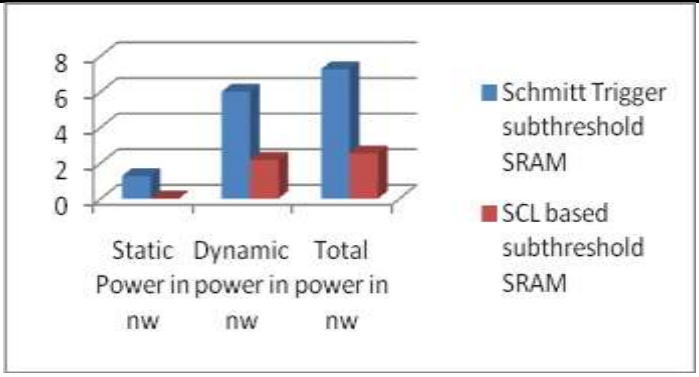
Figure: 3.6 Fall time Delay is 0.02ns

IV RESULT ANALYSIS

Comparison of power & delay

Table 1.1 Power Analysis

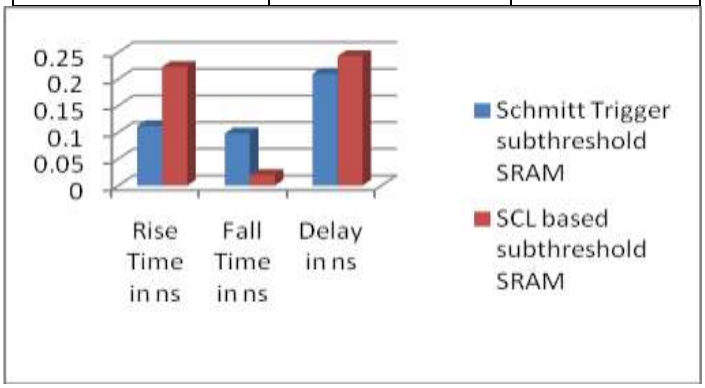
Power analysis	Schmitt Trigger sub threshold SRAM	SCL based sub threshold SRAM
Static Power (nw)	1.2721	**0.01355**
Dynamic power (nw)	5.9972	**2.16829**
Total power (nw)	7.2583	**2.545**



Comparison of delay & analysis

Table 1.2 Delay Analyses

Delay analysis	Schmitt Trigger sub threshold SRAM	SCL based sub threshold SRAM
Rise Time in ns	0.112	**0.223**
Fall Time in ns	0.098	**0.02**
Delay in ns	0.21	**0.243**



Comparative analysis of power Delay product

Table 1.3 Power Delay product Analyses

power delay product	Schmitt SRAM	SCL SRAM
Static Power(nW)	0.142	**0.00302**
Dynamic power(nW)	0.5877	**0.0433**
Total power(nW)	1.5242	**0.6184**

V CONCLUSION

From the above table 1.1,1.2& 1.3 ,The analysis of power, delay, power delay product is estimated. Performance is analyzed under sub threshold operation. The functionality & performance of Schmitt trigger based SRAM and SCL based SRAM is compared and the results showed as below. The power factor is reduced by 35% in overall power, and the delay is increased by 13%.Finally the power delay product reduced by a factor of 40.55%.

From the results it indicated that SCL based SRAM is better in power, where the delay is moderately increasing . But there is a drastic variation in PDP. Therefore SCL based SRAM designs are applicable for emerging technologies, where the Power is the primary issue and delay is the secondary constraint in the memory models.

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