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A TECHNICAL REVIEW ON LOW POWER VLSI ARITHMETIC CIRCUITS

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Abstract: Low power has become a topic of discussion in today's electronic world. Along with area and performance, power dissipation has also become an important parameter for efficiency. The performance of a circuit is often affected by the speed arithmetic components, hence it is crucial to escalate the speed of the arithmetic components. Hence for designing a circuit it is important to keep in mind two important aspects, high speed and low power.

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I INTRODUCTION

Arithmetic circuits find many applications in architectures proposed for signal and image processing. As the complexity of Digital Signal Processing (DSP) architectures is higher, low power design techniques are necessary. For most applications in arithmetic circuits we have to look for maximizing the speed or throughput. The most usual method adopted to reduce power consumption is by using CMOS circuit, and this is because it dissipates less power than other existing components. Technology, circuit design style, algorithm and architecture are the four elements that effect power dissipation in CMOS circuits. In this paper we are going to discuss about 3 adders by comparing their area and delay product results.

In most of the portable devices to obtain low power we often have to compromise on the parameter of time. When we come across most of the signal processing algorithms, we can find that multiplication is one of the elemental operations used. Multipliers usually consume large area, and they have a long latency and also consume considerable power. Therefore it is important to design the multipliers with low power. Many at times to evaluate the performance of a circuit, performance of multipliers are evaluated because of the fact that multipliers are the slowest and the most area occupying elements in the system. Therefore, revising the speed and area of multipliers is an important obstacle to ponder about. But area and speed are complimenting one another, as when speed is improved automatically area will increase. As a result, depending on the parameters of area and speed multipliers are designed.

II ADDERS

Full Adder (FA) is one of the most widely used adder circuits in processing architectures. Decimal adder is the important component of ALUs designed for business and commercial applications. They are the key elements since they have an important role in any circuit and represent the overall performance of the system. These adders should be designed very carefully in the interest to reduce delay and power dissipation of processing architecture. FA designs using single logic style for both sum and carry have certain disadvantages. FA using complementary pass logic suffers from threshold voltage drop problem and FA using CMOS transistors and transmission gates have poor driving capability. The adders we have selected to study about are, ripple carry adder, carry look ahead adder and carry select adder.

A. Ripple carry adder (RCA):

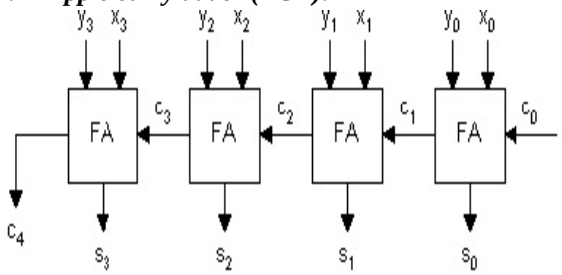

Figure 1: Ripple Carry Adder

A ripple carry adder is designed by connecting multiple full adders in a sequence. Here the carry out of one full adder is given in as the carry in of the successive most significant bit of full adder. It got the name ripple carry adder as it ripples each and every carry bit to the next stage. Ripple carry adder is not preferred for large bit numbers, as it won't be efficient as hat for smaller bits. A deprivation of this adder is that the delay increases along with the bit length. In ripple carry adder the worst-case delay happens when a carry signal ripples through every stages of the adder chain from the least significant bit to the most significant bit. It has advantages such as that it is easy to understand and also has a simple design hence implementation is easier.

B. Carry Select adder (CSLA):

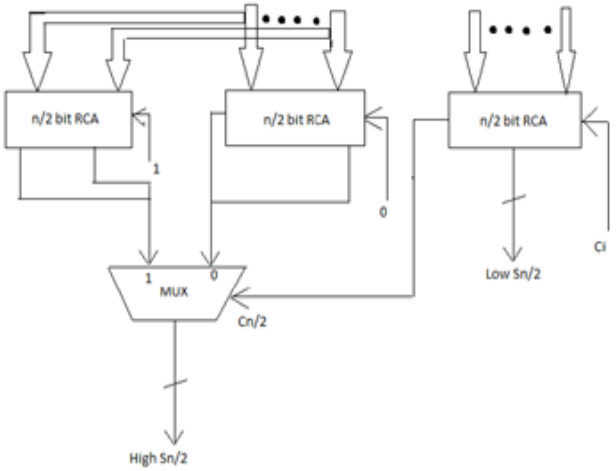

Figure 2 : Carry Select Adders

Carry select adders are constructed using multiple ripple carry adders and a multiplexer. They are used for adding two n-bit numbers. It computes (n+1) bits for two n- bit numbers. Carry look ahead adders are easier to implement and also faster. Each carry select block has number of bits which can be either uniform or varying. Generally multiplexers are used to propagate carries. It is preferable to use carry select adder when smaller number of bits are to be considered.

C. Carry Look ahead Adder (CLA):

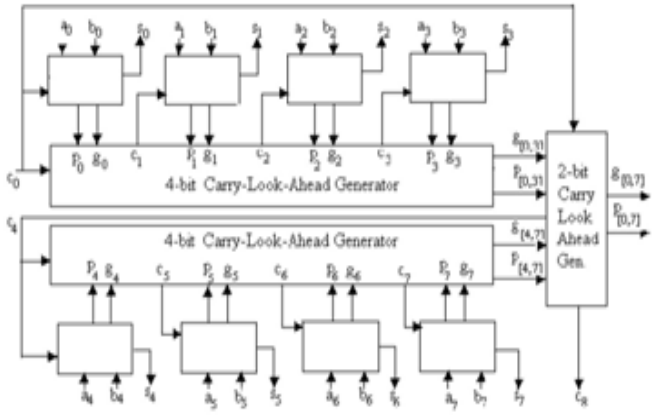

Figure 3 : Carry Look ahead adder

A carry-look ahead adder is a type of adder which has numerous applications in digital logic and it enhances the speed by minimizing the quantity of time required to verify the carry bits. In ripple carry adders, the factor that influences the time is the carry propagation time [3]. Therefore, reducing the carry propagation delay is very important. And this delay is reduced by minimizing the number of gates through which the propagation of carry signal occurs. It uses the principle of generating and propagating carriers.

Propagate block/generate block, a sum generator, a carry generator are the different parts of this adder [4].

D. Analysis of adders:

Here we can see the comparison of three different adders that is, Ripple Carry Adders, Carry Select Adders and the Carry Look Ahead Adders. The core intention out of this paper is to find out the time and power relationship between different adders which will enable us to have a better understanding of using which adder in which type of situation during design process. We have tabulated the area an delay values of the three adders that we have discussed here.

Table 1 : Area Delay Product

Adder	Area values	Delay values	Area delay product
Ripple carry adder(RCA)	7n	2n	14n
Carry select adder (CSLA)	14n	$2.8(n)^{1/2}$	$39.6(n)^{3/2}$
Carry look ahead adder(CLA)	4n	$4\log_2 n$	$16n\log_2 n$

We can bring out the following conclusions from the above table:

1. When comparing the area and complexity of the architecture we can say that the ripple carry adder(RCA)is the most efficient of the three adders and the carry select adder(CSLA) is the least efficient as its area is more compared to the other two adders and hence the complexity will also increase. [2].
2. When considering the time consuming component, carry select adder (CSLA) is the quickest among the three adders hence will have the shortest delay, followed by Ripple carry adder (RCA) because of it limitation of time consuming carry propagation[2].

Here we have found the area delay product which gives as a proper understanding on the efficiency of theses adders. If we concentrate on these adders that we have considered, from all the adders which we discussed above ripple carry adders and carry select adders are in a way opposite to each other. This can be seen very clearly that

ripple carry adders have a smaller area and speed is less, on the contrary carry select adders have high speed and not just that, the speed is almost twice the speed of ripple carry adder and also they occupy a larger area. When drawing attention to carry look ahead adder (CLA) we can see that it has a balance between the two components area and time. Therefore, it can be clearly stated that from the adders discussed above, carry look ahead adder has the minimum area and delay product. Hence we should use carry look ahead adders when we need to consider improvement with both area and time.

III MULTIPLIERS

Multipliers have their most applications in the field of DSP, Image processing architecture and microprocessors. Here we are discussing about parallel multipliers. The crucial parameter of his multiplier is the number of partial products o be added. As multipliers have high switching and critical computations, when compared to the other counterparts before designing a multiplier the designers take care of parameters such as low power dissipation and better speed.

Here we are going to discuss about the two most widely used multipliers. The Wallace tree multiplier and the Booth's Multiplier.

A. The Wallace tree Multiplier

The Wallace tree multiplier was devised by a computer scientist Chris Wallace in the year 1964.It is considered to have much better performance than a simple array multiplier. When considering unsigned multiplication, to form the results we add n shifted copies of the multiplicand [6]. However, the Wallace tree is much complicated because of the use of numerous adders an also the wiring of Wallace tree is not very regular and quite complex. Therefore designers often avoid using Wallace trees when the parameters of complexity and area are considered. Wallace tree is considered to be very fast but limitations are when it comes to irregularity and complexity along with area component. Wallace tree design is often avoided for low power applications as the wiring is not regular and also since it is complex they are avoided by designers[1][5].

The given block diagram indicates the intermediate state reductions of the multipliers which are being done by Carry save adders and half adders. The final step additions are being done by a Carry Look Ahead Adder. The designed flow diagram is of a Generic Wallace tree as after generating the flow diagram for 8-bit × 8-bit we generalized the algorithm for n-bit[2].

B. The Booth's Multiplier

Wallace tree Multiplier is efficient when we compare it with the Carry save method but the problem arises when we consider the wiring irregularity and complexity of Wallace tree. When multiplier bits gets more than 32-bits, then the requirement of logic gates also increases and along with that more interconnecting wires will also increase which automatically makes chip design larger and also slows down operating speed. In order to cope up with these limitations a Booth multiplier can be used. There are different modes by which Booth multiplier can be used. These modes are radix-2, radix-4, radix-8 etc. Here we have decided to use Radix-4 Booth's Algorithm .This is due to the fact that, the number of Partial products is reduced to n/2 in radix-4 Booth's algorithm [2].

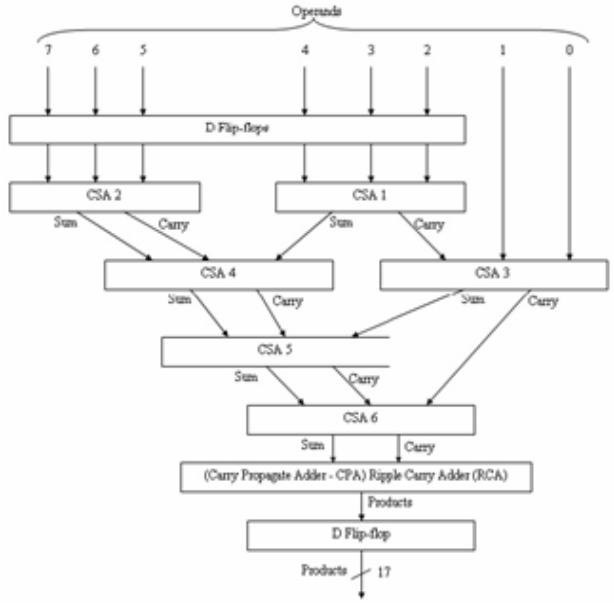

Figure 4: Wallace tree multiplier

Booth multiplier technique is mostly used to increase speed. This can be done by reducing the number of partial products to half. Here we are using an 8-bit booth multiplier, so we have to add only four partial products.

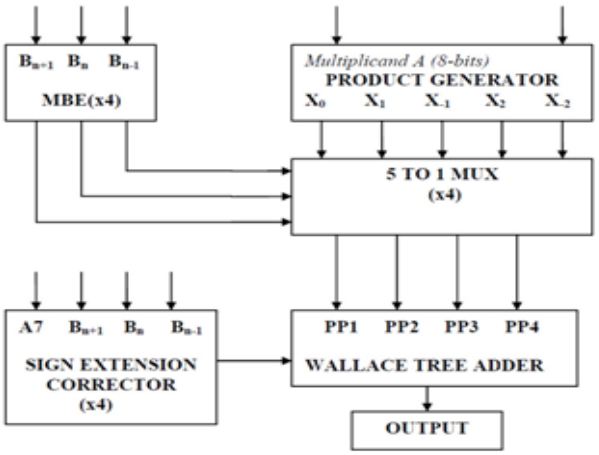

Figure 5: Booth's Multiplier

C. Analysis of Multipliers

Here we are comparing two multipliers which are Wallace tree multiplier and Booth's multiplier. These two multipliers are compared on the basis of the parameters of speed and power. Below we have analyzed Wallace Tree Multipliers and Booth Multiplier (Radix-2 and Radix-4) and

analyzed their speed and power consumption. We have discussed the number of slices, Number of 4-input LUTs, number of bonded inputs and outputs and also power.

Table 2: Wallace Tree Multiplier

Parameters	Values
Number of Slices	69
Number of 4-input LUTs	125
Number of bonded inputs	32
Number of bonded outputs	32
Power	81mW

Table 3: Booth Multiplier (Radix-2)

Parameters	Values
Number of Slices	72
Number of 4-input LUTs	130
Number of bonded inputs	32
Number of bonded outputs	32
Power	114mW

Table 4: Booth Multiplier (Radix-4)

Parameters	Values
Number of Slices	96
Number of 4-input LUTs	178
Number of bonded inputs	32
Number of bonded outputs	32
Power	76mW

When we compare the above values with each other we can conclude that the worst case multiplier consuming the most power among the three is Radix -2 booth. The other two multipliers which are the Wallace Tree multiplier and Booth Multiplier Radix-4, they have nearly same amount of delay and also Radix-4 Booth consumes lesser power when compared to the other. Therefore we can reach to a conclusion that Booth Radix-4 Multiplier is preferred for the situations that require low power applications [2].

IV CONCLUSION

Here we had discussed about three adders and two multipliers .In the process we compared them in the aspects of time, area, area-delay product etc. in order to use the best according to situations. After the comparison of the adders we came to a conclusion that Carry Select Adders (CSA) is best suited for situations where the only criteria of consideration are speed. When coming to Low Power applications Ripple carry Adders (RCA) are to be considered. But we cannot keep aside the fact that the Carry Look Ahead Adder had the least Area-Delay product that tells us that it is to be used for situations where we can take into consideration both speed and low power. Since we need a proper balance between both speed and low power.

When we analyzed the Multipliers we could study different Multipliers such as Wallace Tree multiplier and Booth Multipliers. We found that among parallel multipliers and serial multipliers, parallel multipliers are much better than the serial multipliers and this is due to less area consumed by parallel multipliers and hence it will have less power consumption. When comparing Radix-2 and Radix-4 booth multipliers, radix-4 consumes less power than radix-2 and this is because radix-4 uses only half number of iterations than radix-2. Since from the table we found that Wallace tree have nearly same delay as that of radix-4 multipliers and where as consuming a little more power than the former. By using proper recording schemes the power efficiency of the system can be improved.

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BIOGRAPHY

Ms. Merrin Mary Solomon is currently pursuing M.Tech in Electronics and Communication Engineering from Amity University Haryana. She completed her B.Tech from Nehru Institute of Engineering and Technology Coimbatore under Anna University Chennai. Her B.Tech projects were done in the area of Image

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